REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, the withdrawn claims have been maintained. Moreover, claim 22 has been cancelled without prejudice or disclaimer, and new claim 32 substituted therefor. Claim 32 defines a substrate for mounting semiconductor devices thereon, having an insulating supporting member and plural sets of wirings, with this substrate further including a semiconductor device mounting region and a resin-sealing semiconductor package region outside of the semiconductor device mounting region. Claim 32 further recites that the plural sets of wirings comprise a predetermined wiring pattern including wire-bonding terminals and external connection terminals, with the wire-bonding terminals being provided in the semiconductor package region and the external connection terminals being provided in the semiconductor device mounting region. Claim 32 also recites that the substrate includes a plurality of the semiconductor device mounting regions, with the plurality of semiconductor device mounting regions respectively having blocks of the wirings, each having a same pattern. In connection with new claim 32, note, illustratively and not to be limiting, Figs. 11c-11g. In light of new claim 32, claim 23 has been cancelled without prejudice or disclaimer, and claim 24, including dependency thereof, has been amended. Moreover, dependencies of claims 25 and 31 have been amended, in light of new claim 32; and claim 26 has been cancelled without prejudice or disclaimer.

In addition to new claim 32, Applicants are adding new claims 33-37 to the application. New independent claim 33 defines a substrate for mounting semiconductor devices thereon, having an insulating supporting member and plural

sets of wirings, and wherein the wirings form a predetermined wiring pattern including a wire-bonding terminal and an external connection terminal, the external connection terminal being provided only inside of the wire-bonding terminal. Claims 34 and 35, each dependent on claim 33, respectively recites that the substrate includes a plurality of the wiring patterns, which include a plurality of the wirings arranged in rows and columns; and recites that the wire-bonding terminal includes a nickel layer and a gold plate layer on its surface. Claim 36, dependent on claim 33, recites that the external connection terminal is one of a plurality of external connection terminals, exposed on a surface of the insulating supporting member, on an opposite side to which the semiconductor device is mounted, with these terminals being arranged in a grid pattern at positions corresponding to the semiconductor device mounting region and the semiconductor package region. New claim 37 defines a semiconductor package produced by a specified method and corresponds to claim 31, but recites that the substrate is the substrate according to claim 33.

The finality of the Restriction Requirement, as set forth on page 2 of the Office Action mailed November 24, 2003, is noted. The withdrawn claims are being retained in the above-identified application, subject to the filing of a Divisional application directed to the subject matter thereof or subject to taking further action in connection therewith in the above-identified application, consistent with 37 CFR § 1.144.

Applicants respectfully submit that all of the claims being considered on the merits in the above-identified application patentably distinguish over the teachings of the references applied by the Examiner in the Office Action mailed November 24, 2003, that is, the teachings of Japanese Patent Document

No. 2-153542 to Tatsuo and Japanese Patent Document No. 59-208756 to Katsuhiko, under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a semiconductor substrate as in the present claims, having the semiconductor device mounting region and resin-sealing semiconductor package region outside of the semiconductor device mounting region, with plural sets of wirings including a predetermined wiring pattern having wire-bonding terminals and external connection terminals, and wherein the wire-bonding terminals are provided in the semiconductor package region and the external connection terminals are provided in the semiconductor device mounting region, the substrate including a plurality of the semiconductor device mounting regions respectfully having blocks of the wirings which each have a same pattern. See claim 32.

In addition, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a substrate for mounting semiconductor devices thereon as in the present claims, having the plural sets of wirings, and wherein the wirings form a predetermined wiring pattern including wire bonding and external connection terminals, the external connection terminal being provided only inside of the wire bonding terminal. See claim 33.

Moreover, it is respectfully submitted that these applied references would have neither taught nor would have suggested such a semiconductor package as in the present claims, produced by a method including, inter alia, mounting a semiconductor device on each of plural semiconductor device mounting regions of

the aforementioned substrate according to claim 33 or according to claim 32. See claims 31 and 37.

Furthermore, it is respectfully submitted that these applied references would have neither taught nor would have suggested such a substrate for mounting semiconductor devices thereon as in the present claims, having features as discussed previously in connection with independent claims 32 and 33, and, in addition, having further features such as (but not limited to) wherein the wire-bonding terminals include a nickel layer and a gold plate layer on its surface (see claims 24 and 34); and/or wherein the substrate includes a plurality of the wiring patterns comprised of a plurality of the wirings arranged in rows and columns (see claim 34); and/or wherein the external connecting terminals are exposed on a surface of the insulating supporting member, on an opposite side on which the semiconductor device is mounted, with the external connection terminals being arranged in a grid pattern at positions corresponding to the semiconductor device mounting region and the semiconductor package region (see claims 25 and 36).

Thus, according to the present invention as claimed herein, the external connection terminals are provided inward of the wire-bonding terminals, whereby the package structure can be simplified and the package itself can be miniaturized. Moreover, by using the substrate according to the present invention, wiring between the semiconductor device and the substrate can be provided by wire bonding, so that a large number of relatively small-sized semiconductor packages can be produced in a simple process, at a very low cost.

Tatsuo discloses a technique for manufacturing a high-dimensional accuracy and high-quality thin integrated circuit device suitable for an IC card. According to

Tatsuo, an insulative bonding agent 12 is applied on most of one surface 11a of a metallic thin plate 11 excepting connecting parts of the one surface 11a with gold wires 14, and an integrated circuit element 13 is mounted and fixed through this bonding agent. Note Figs. 1(a)-(d) of Tatsuo. After fixing the integrated circuit element 13, the element 13, the wires 14 and the side of the one surface 11a of the plate 11 are coated with a sealing resin 15, and subsequently unnecessary parts of the plate 11 are removed to form the plate 11 in a desired configuration.

As can be seen, for example, in Fig. 6 of Tatsuo, the external connection terminals are provided outside the semiconductor device mounting region, and outside the wire-bonding terminals. It is respectfully submitted that the teachings of Tatsuo would have neither disclosed nor would have suggested, and, in fact, would have taught away from, the presently claimed substrate and semiconductor package, wherein the wire-bonding terminals are provided in the semiconductor package region and the external connection terminals are provided in the semiconductor device mounting region, as in claim 32; or wherein the external connection terminal is provided only inside of the wire-bonding terminal, as in claim 33.

The increased size of the package of Tatsuo, due to the external connection terminals being outside the wire-bonding terminals and being outside the semiconductor mounting region, can be appreciated when comparing, for example, Fig. 11g of Applicants' disclosure with Fig. 6 of Tatsuo. That is, the present invention utilizes a chip-size packaging by providing the external connection terminal inside of the wire-bonding terminal. Such feature of the present invention would have neither been disclosed nor would have been suggested by Tatsuo.

It is respectfully submitted that the additional teachings of Katsuhiko would not have rectified the deficiencies of Tatsuo, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Katsuhiko discloses a semiconductor device package which is excellent in heat radiation and suitable for automated manufacturing. The structure includes a gold plating 12 (see Fig. 2A), nickel plating 13 and gold plating 14, each of specified thickness, laminated on an iron substrate 11 of specified thickness. A semiconductor chip 15 (note Fig. 2B) is mounted on a portion 11g (note Fig. 5A) and connected to external electrodes 17, 18 on the portions 11h, 11i, with transfer molding with epoxy resin 20 being carried out. The iron substrate is removed by etching with $FeCl_3$ solution from the back surface 11a to complete a leadless type package 21.

As can be appreciated from, for example, Fig. 4B of Katsuhiko, according to the structure described therein the external connection terminals are outside of the semiconductor mounting region and fall directly beneath the wire-bonding terminal. It is respectfully submitted that the disclosure of Katsuhiko, by itself or together with the disclosure of Tatsuo, would have taught away from the presently claimed substrate including, inter alia, wherein the external connection terminal is provided only inside of the wire-bonding terminal; and/or wherein the wire-bonding terminals are provided in the semiconductor package region and the external connection terminals are provided in the semiconductor device mounting region, and advantages thereof in providing a chip-size package; and/or the other features of the present invention as discussed previously, and advantages thereof.

The Information Disclosure Statement submitted April 5, 2004, in connection with the above-identified application, is noted. If this Information Disclosure

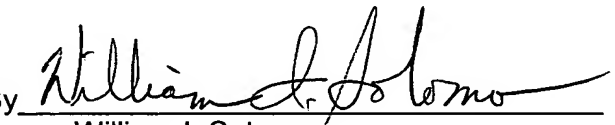
Statement is not in the file of the above-identified application when the Examiner takes up the above-identified application for consideration, the Examiner is respectfully requested to contact the undersigned for a further copy of such Information Disclosure Statement, if necessary. The Examiner is thanked in advance for complying with this request.

In view of the foregoing, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 566.43481CC4), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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